# ROBUST CALCULATION OF CROSSTALK DELAY CHANGE IN INTEGRATED CIRCUIT DESIGN

## ABSTRACT

A method of delay change determination in an integrated circuit design including a stage with a victim net and one or more aggressor nets capacitively coupled thereto, the method comprising: determining a nominal (noiseless) victim net signal transition; determining a noisy victim net signal transition; and determining a delay change based upon nominal and noisy victim signal transition arrival times at a victim net receiver output.